IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): MUTHUKUMARASWAMY and ROSTOKER

Title: MULTIMEDIA INTERFACE HAVING A PROCESSOR AND RECONFIGURABLE LOGIC (As Amended Herewith)

PRELIMINARY AMENDMENT

IN THE CLAIMS

Cancel all of the existing claims (1-22), and ***add*** the following (23-xx)

23. Multimedia interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip; and

a block of media processor with a virtual instruction set capable of implementing a variety of multimedia algorithms incorporated on the IC chip separately from the reconfigurable logic block.

24. The multimedia interface, according to claim 23, further comprising audio and/or video CODEC incorporated on the IC chip.

25. The multimedia interface, according to claim 23, further comprising a phase locked loop (PLL) circuitry incorporated on the IC chip.

26. The multimedia interface according to claim 23, further comprising a programmable, fast serial interface core incorporated on the IC chip.

27. The multimedia interface according to claim 23, further comprising a programmable CPU interface core incorporated on the IC chip.

28. The multimedia interface according to claim 23, further comprising a programmable memory interface (PMI) core incorporated on the IC chip.

29. Multimedia interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a media processor block incorporated on the IC chip; and

audio and/or video CODEC incorporated on the IC chip for interfacing to external analog signals.

30. Multimedia interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a media processor block incorporated on the IC chip; and

phase locked loop (PLL) circuitry incorporated on the IC chip to reduce skew within various blocks within the IC chip.

31. Multimedia interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a media processor block incorporated on the IC chip; and

a programmable, fast serial interface core incorporated on the IC chip.

32. Multimedia interface according to claim 31, wherein:

the programmable, fast serial interface core is incorporated within the reconfigurable logic block.

33. Multimedia interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a media processor block incorporated on the IC chip; and

a programmable CPU interface core incorporated on the IC chip.

34. Multimedia interface according to claim 33, wherein:

the programmable CPU interface core is incorporated within the reconfigurable logic block.

35. Multimedia interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a media processor block incorporated on the IC chip; and

a programmable memory interface (PMI) core incorporated on the IC chip.

36. Multimedia interface according to claim 35, wherein:

the programmable memory interface core is incorporated within the reconfigurable logic block.

37. Multimedia interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a media processor block incorporated on the IC chip; and

at least one additional core selected from the group consisting of

audio and/or video CODECs for interfacing to external analog signals;

phase locked loop (PLL) circuitry to reduce skew within various blocks within the IC chip;

a programmable, fast serial interface core;

a programmable CPU interface core;

a programmable memory interface (PMI) core; and

further comprising power-down circuitry, in combination with one or more of these additional cores, incorporated on the IC chip to provide power and/or processing savings when a given one of the cores is not in use.

38. Signal processing interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a RISC core incorporated on the IC chip; and

audio and/or video CODEC for interfacing to external analog signals incorporated on the IC chip.

39. Signal processing interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a RISC core incorporated on the IC chip; and

phase locked loop (PLL) circuitry incorporated on the IC chip to reduce skew within various blocks within the IC chip.

40. Signal processing interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a RISC core incorporated on the IC chip; and

a programmable, fast serial interface core incorporated on the IC chip.

41. Signal processing interface according to claim 40, wherein:

the programmable, fast serial interface core is incorporated within the reconfigurable logic block.

42. Signal processing interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a RISC core incorporated on the IC chip; and

a programmable CPU interface core incorporated on the IC chip.

43. Signal processing interface according to claim 42, wherein:

the programmable CPU interface core is incorporated within the reconfigurable logic block.

44. Signal processing interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a RISC core incorporated on the IC chip; and

a programmable memory interface (PMI) core incorporated on the IC chip.

45. Signal processing interface according to claim 44, wherein:

the programmable memory interface core is incorporated within the reconfigurable logic block.

46. Signal processing interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a RISC core incorporated on the IC chip; and

at least one additional core selected from the group consisting of

audio and/or video CODEC for interfacing to external analog signals;

phase locked loop (PLL) circuitry to reduce skew within various blocks within the IC chip;

a programmable, fast serial interface core;

a programmable CPU interface core;

a programmable memory interface (PMI) core; and

further comprising power-down circuitry, in combination with one or more of these additional cores, incorporated on the IC chip to provide power and/or processing savings when a given one of the cores is not in use.

IN THE SPECIFICATION

Replace the original title, at page 1, line 0 ("MULTIMEDIA FPGA") with:

-- MULTIMEDIA INTERFACE HAVING A PROCESSOR AND RECONFIGURABLE LOGIC --

(and please delete the docket number at the extreme top left of page 1)

Replace the paragraph at page 1, lines 2-6, with:

-- This application is a continuation of commonly-owned, copending U.S. Patent Application No. 09/166,499 filed 10/05/98 (now USP 6,279,045, issued 8/21/01), which is a continuation-in-part of commonly-owned, copending U.S. Patent Application No. **60/068,851** filed 12/29/97, and of commonly-owned, copending U.S. Patent Application No. **60/068,852** filed 12/29/97, all of which are incorporated in their entirety by reference herein. --

REMARKS

The Inventor's name

The co-inventor's name is MUTHUKUMARASWAMY, not MUTHUJUMARASWA**TH**Y.

The Declaration (***copy enclosed***) was signed correctly as "MUTHUKUMARASWAMY"

Please ensure that this inventor's name appears correctly spelled in all correspondence.

The Title

The title is amended herewith.

The Parent Case (09/166,499)

The Parent Case is issuing. The main reference used against the claims of the parent case was Gilson (USP 5,600,845). As a convenience to the Examiner, the allowed claims of the parent case, are appended ("APPENDIX") hereto:

Newly-Presented Claims

The following comments are presented as a aid (guide) to the Examiner.

Newly-presented **claim 23** recites " a block of media processor with a virtual instruction set capable of implementing a variety of multimedia algorithms incorporated on the IC chip separately from the reconfigurable logic block." Applicant believes that this is not shown in Gilson.

It should be noted that the term "media processor", rather than "multimedia processor" is used in this and some of the other claims presented herewith, because the specification mainly uses "media processor".

Main Claim 3 of the allowed/issuing parent case (see APPENDIX) recites:

3. Multimedia interface, comprising:
   an integrated circuit (IC) chip;
   a block of reconfigurable logic incorporated on the IC chip; and

a multimedia processor block incorporated on the IC chip separately from the reconfigurable logic;

further comprising at least one functional block selected from the group consisting of:

audio and/or video CODECs for interfacing to external analog multimedia signals;

phase locked loop (PLL) circuitry to reduce skew within various blocks within the IC chip and to synchronize to off-chip clock circuitry;

a programmable, fast serial interface core;

a programmable CPU interface core;

a programmable memory interface (PMI) core; and

power-down circuitry, in combination with one or more of these additional cores.

This claim 3 includes a reconfigurable logic block, multimedia processor block, and at least one additional functional block selected from a group of different functional blocks.

Newly-presented **claims 29, 30, 31, 33, 35** recite each of these five combinations, although certain words are deleted, and the functional block is specifically recited to be "incorporated on the IC chip". Additionally, these claims do not recite that the "media processor block" is incorporated "separately from the reconfigurable logic" because this language was apparently not afforded much patentable weight in the parent case.

Further, newly-presented **claim 29** recites "CODEC" rather than "CODECs" as recited in claim 3 of the parent case. A combination of an encoder and a decoder is usually called a "CODEC". The use of the term "CODECs" was a grammatical choice.

Newly-presented dependent **claims 32, 34 and 35** recite that the interface core is incorporated within the reconfigurable logic block. See page 14, lines 6-9 of the Specification ("the following configurable portions of the logic block"), and Figure 2. In newly-presented **claim 36**, the programmable memory interface core is incorporated within the reconfigurable logic block.

Newly-presented **claim 37** is similar to claim 3 of the parent case. However, this claim specifically requires a combination of the power-down circuitry and one or more of the additional cores. Note that the "additional cores" include "CODEC" and "PLL". See page 9, lines 14-17 of the specification.

Newly-presented **claims 38-46** are similar to newly-presented **claims 29-37**, except that these claims recite a "RISC core" rather than a "media processor block". Compare claim 15 of the parent case.

For the applicant,

Gerald E. Linden 8/14/01

Gerald E. Linden 30,282 date

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ADDITIONAL SHEET SHOWING CHANGES MADE TO THE SPECIFICATION

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